IN THE CLAIMS

Please cancel Claims 1-2 without prejudice and amend Claim 3 as follows:

1-2 (Cancelled)

3. (Currently Amended) A receiver (1) comprising ~~the~~ a DC-offset correction circuit (I1, Q1)~~.~~, said DC-offset correction circuit comprising:

a DC-offset control loop embodied by:

a summing device having a signal path input, a DC control input, and a summing output; and

an offset determining means coupled between the summing output and the DC control input of the summing device; and

a DC blocking circuit coupled to the summing output of the summing device and having a DC blocking output for providing an offset corrected output signal ~~according to claim 1, characterised in that~~ wherein the receiver (1) comprises channel filter means (DFI, DFQ) coupled between the summing device (9-1, 9-2) and the DC blocking circuit (17-1, 17-2).

4. (Original) The receiver (1) according to claim 3, characterised in that the channel filter means comprise analog or digital filters (DFI, DFQ), in case of an analog or digital implementation respectively of said channel filter means.

5. (Previously Presented) The receiver (1) according to one of the claims 3, characterised in that the receiver is a quadrature receiver (1).

6. (Previously Presented) The receiver (1) according to one of the claims 3, characterised in that the receiver is a low-IF receiver, or a zero-IF receiver.

7. (Previously Presented) The receiver (1) according to one of the claims 3, characterised in that the receiver is a double conversion receiver (1).

8. (Previously Presented) The receiver (1) according to one of the claims 3, characterised in that the receiver (1) is provided with analog to digital (AD) converters (13-1, 13-2) and/or digital to analog (DA) converters (16-1, 16-2; 20).

9. (Previously Presented) The receiver (1) according to one of the claims 3, characterised in that the receiver (1) is provided with switchable means (3, 5, 7-1, 7-2).